What is claimed is:

1. A method of forming a capacitor in a substrate comprising the steps of:
etching a trench in said substrate;
forming a first capacitor plate by diffusing a dopant into said substrate;
depositing a first conformal dielectric layer on an interior surface of said trench;
depositing a first conductive storage plate on an interior surface of said first dielectric layer;
depositing a second conformal dielectric layer on an interior surface of said first conductive storage plate;
etching directionally through said second dielectric layer and said first storage plate to expose a substrate contact surface of said first capacitor plate whereby upper and lower edges of said first storage plate are exposed;
forming an insulator covering said exposed upper and lower edges of said first storage plate;
depositing a second capacitor plate on an interior surface of said second dielectric layer, to make electrical contact with said substrate contact surface;
forming a third dielectric layer on exposed interior surfaces of said second capacitor plate;
removing said insulator covering said exposed upper edge of said first storage layer, thereby exposing said upper edge of said first storage plate; and
depositing a second conductive storage plate abutting said third dielectric layer, thereby establishing electrical contact between said first and second conductive storage plates, which are separated from said first and second capacitor plates by said first, second and third dielectric layers.

2. A method according to claim 1, further comprising a step, before said step of forming a first capacitor plate of, forming a dopant protective layer having an outer

nitride layer on the interior surface of said trench;
depositing resist, recessing said resist to a capacitor top position below a substrate surface;
stripping said outer nitride layer above said capacitor top position;
stripping said dopant protective layer below said capacitor top position, thereby exposing said substrate.

3. A method according to claim 2, in which said substrate is a silicon wafer;
said dopant protective layer comprises a layer of oxide adjacent to said substrate, a layer of nitride, a layer of poly and an outer layer of nitride; and, after said step of stripping said outer layer, further comprising a step of oxidizing said layer of poly.

4. A method according to claim 1, further comprising a step of performing a bottle etch before said step of diffusing dopant into said substrate, thereby forming an upper portion of said trench having a first width and a lower portion of said trench having a second width greater than said first width.

5. A method according to claim 1, further comprising a step of forming a layer of hemispherical grained silicon on an interior surface of at least one silicon layer.

6. A method according to claim 1, in which said step of forming a third dielectric layer is performed by thermal nitridation.

7. A method according to claim 4, further comprising, after said step of forming said first storage plate, a step of removing material from said first storage plate from said upper portion of said trench, thereby forming a contact edge of said first storage plate.

8. A method according to claim 7, in which said second storage plate makes contact

with said first storage plate at said contact edge, disposed outside said first width of said upper portion of said trench.

9. A method according to claim 1, further comprising a step of forming a transistor having one electrode connected to said storage plate of said capacitor and a second electrode connected to a cell electrode, thereby forming a DRAM cell.

10. A method according to claim 9, further comprising a step, before said step of forming a first capacitor plate of, forming a dopant protective layer having an outer nitride layer on the interior surface of said trench;
depositing resist, recessing said resist to a capacitor top position below a substrate surface;
stripping said outer nitride layer above said capacitor top position;
stripping said dopant protective layer below said capacitor top position, thereby exposing said substrate.

11. A method according to claim 10, in which said substrate is a silicon wafer;
said dopant protective layer comprises a layer of oxide adjacent to said substrate, a layer of nitride, a layer of poly and an outer layer of nitride; and, after said step of stripping said outer layer, further comprising a step of oxidizing said layer of poly.

12. A method according to claim 10, further comprising a step of performing a bottle etch before said step of diffusing dopant into said substrate, thereby forming an upper portion of said trench having a first width and a lower portion of said trench having a second width greater than said first width.

13. A method according to claim 12, further comprising, after said step of forming said first storage plate, a step of removing material from said first storage plate from said

upper portion of said trench, thereby forming a contact edge of said first storage plate.

14. A method according to claim 13, in which said second storage plate makes contact with said first storage plate at said contact edge, disposed outside said first width of said upper portion of said trench.

15. A capacitor formed in an integrated circuit substrate comprising:
a trench etched in said substrate;
a first capacitor plate formed by diffusing a dopant into said substrate outside said trench;
a first conformal dielectric layer deposited on an interior surface of said trench;
a first conductive storage plate formed on an interior surface of said first dielectric layer;
a second conformal dielectric layer deposited on an interior surface of said first conductive layer;
a second capacitor plate deposited on an interior surface of said second dielectric layer, said second capacitor plate extending into the bottom of said trench, passing through said second dielectric layer, said first storage plate and said first dielectric layer and making electrical contact with said first capacitor plate, said second capacitor plate being isolated from said first storage plate;
a third dielectric layer formed on exposed interior surfaces of said second capacitor plate; and
a second conductive storage plate deposited on an interior surface of said third dielectric layer and in electrical contact with said first conductive storage plate in an upper region of said trench above said second capacitor plate, said first and second conductive storage plates being separated from said first and second capacitor plates by said first, second and third dielectric layers.

16. A capacitor according to claim 15, in which said trench has a lower portion containing said first and second conductive storage plates and an upper portion

connecting said lower portion to a substrate surface, in which said upper portion has an upper width and said lower portion has a lower width greater than said upper width.

17. A capacitor according to claim 16, in which said second storage plate makes contact with said first storage plate at a contact edge disposed outside said first width of said upper portion of said trench.

18. A capacitor according to claim 15, further comprising a transistor having one electrode connected to said storage plate of said capacitor and a second electrode connected to a cell electrode, thereby forming a DRAM cell.

19. A capacitor according to claim 18, in which said trench has a lower portion containing said first and second conductive storage plates and an upper portion connecting said lower portion to a substrate surface, in which said upper portion has an upper width and said lower portion has a lower width greater than said upper width.

20. A capacitor according to claim 19, in which said second storage plate makes contact with said first storage plate at a contact edge disposed outside said first width of said upper portion of said trench.